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CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German application DE 102 45 536.8, filed with German Patent Office on September 30, 2002.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Calibration of semiconductor devices using a common calibration reference

The invention relates to the calibration of interface devices in semiconductor devices using a calibration reference.

In data bus systems, data lines combined to form a common data bus are used to transmit data signals between a plurality of semiconductor devices. As data transmission rates increase on the data bus, the semiconductor devices effecting access for the purpose of writing to the data bus or reading from the data bus demand narrower tolerances for the interface parameters in order to maintain the integrity of the data signals transmitted to the data bus. A first such interface parameter is the impedance of output drivers (OCD, off chip driver), which a semiconductor device uses to output data signals to data signal lines in the data bus. Another interface parameter is formed by terminations, which terminate the data bus locally in the semiconductor device in order to prevent reflection (OCT, on chip termination).

The interface parameters are subject to production variations and vary both from semiconductor device to semiconductor device and within a semiconductor device from output driver to output driver. In addition, the interface parameters are dependent on installation conditions for the semiconductor device and need to be matched to a configuration of the data bus system. The interface parameters are also subject to variations over time during operation of the semiconductor device. In this case, the variations over time result, by way

of example, from any temperature dependency of the interface parameters or the latter's dependency on an operating voltage for the semiconductor device.

For operation in data bus systems with a high data transmission rate, the semiconductor device's interface parameters are therefore compared with a nominal value by a calibration unit implemented in the semiconductor device at least once before or during startup of the semiconductor device or repeatedly during operation of the semiconductor device and are realigned if required. In this context, the nominal value is ascertained using a calibration reference. For the alignment, both analog and digital methods using state machines and amplifier circuits are known.

For DRAMs (dynamic random access memories) based on the DDR (double data rate) standard, the output drivers can be aligned conventionally by impressing a calibration current via the output drivers' connections, measuring the voltage drop produced by the calibration current across the output drivers, and comparing the measured voltage drop with a nominal value for the voltage drop. For the alignment, the value of a control element for the output driver is set using an entry in a mode register in the DRAM. Such alignment of the output drivers is normally carried out before starting up the semiconductor device in a data bus system in a test laboratory. Matching to specific installation parameters is then not possible.

The calibration reference is provided, by way of example, as a voltage reference or calibration resistor either within the semiconductor device or outside the semiconductor device.

If the calibration reference is arranged inside the semiconductor device, then a particular drawback is the circumstance that a value for the calibration reference actually need to be stipulated at the time at which the semiconductor device is produced. On the other hand, however, it is thus possible to match the interface parameters in terms of a configuration of the data bus system only if the semiconductor device is produced in various series using respectively different values for the calibration reference.

By contrast, an external calibration reference connected to a calibration connection on the semiconductor device allows late stipulation of the value of the calibration reference in a manner matched to the respective data bus system. In addition, the accuracy and, by way of example, further compensation circuits for stabilizing the calibration reference, and also subsequently the system costs, can advantageously be matched to the demands on the data bus system.

Fig. 1 shows a DDR-DRAM 1' having output drivers 6 which can be calibrated using an external calibration reference 5. To make matters simpler, the illustration in this case has been reduced to those components of the DDR-DRAM which are fundamental in this context. The DDR-DRAM 1' has control and address connections 21 for connecting a control and address bus CA, data connections 22 for connecting a data bus formed by data lines DQ, DM, DQS, and a calibration connection 32. The calibration reference 5 is connected to the calibration connection 32. A calibration unit 3 connected to the calibration connection 32 via a calibration path 31 uses the calibration reference 5 to align the output drivers 6.

Fig. 2 shows a plurality of the DDR-DRAMs 1' described with reference to Fig. 1, arranged to form a data bus system. In

this case, each DDR-DRAM 1' has an associated external calibration reference 5.

A method for calibrating fast-switching output drivers outside the test laboratory in an operating environment is described in US 6,330,194 B1 (Thomann et al.). In this case, a group of output drivers, for example the output drivers for a data bus in a DDR-DRAM, is aligned similarly to the result of an alignment for a further calibration driver, which is essentially similar to the data bus output driver. A signal level driven by the calibration driver is aligned with a reference voltage, with the output drivers' load formed by the bus configuration being simulated by switching the output of the calibration driver to a further data line routed parallel to the data bus, for example a data mask line (DM, data mask), during the alignment.

A drawback of known arrangements with external calibration references in systems having a high storage density is the large space requirement for the calibration references as compared with the space requirement in corresponding semiconductor memory devices.

It is therefore an object of the present invention to provide a calibration method for semiconductor devices which reduces the space requirement for calibration references while providing essentially the same quality of calibration as compared with conventional methods. It is also an object of the present invention to provide an operating method for a plurality of calibratable semiconductor devices, and also a semiconductor device and an arrangement of semiconductor devices which respectively permit such a calibration method and operating method.

The calibration method for semiconductor devices which achieves the object is specified in patent claim 1. The operating method for semiconductor devices which achieves the object can be found in patent claim 7. The object is also achieved for a semiconductor device by the features specified in the characterizing part of patent claim 9 and is achieved for a memory module by the features specified in the characterizing part of patent claim 13.

The inventive method for calibrating interface devices in semiconductor devices using a calibration reference which is connected to at least one calibration connection on a semiconductor device thus comprises the following steps:
1) a plurality of semiconductor devices which each have a calibration unit which is connected to the calibration connection via a calibration path which can be switched by a switching unit are provided,
2) an active calibration signal connecting the calibration unit to the calibration connection using the switching unit is respectively generated in a first semiconductor device,
3) the interface devices in the first semiconductor device are calibrated,
4) a passive calibration signal isolating the calibration unit from the calibration connection using the switching unit is generated, and
5) steps 2) to 4) are respectively repeated for all further semiconductor devices.

In line with the inventive method, a plurality of semiconductor devices are accordingly assigned a single calibration reference. The semiconductor devices are aligned in succession, in each case individually, with just the calibration connection on the respective semiconductor device which is currently performing calibration being connected to

the calibration unit by means of an internal switching unit, and the calibration connections on all other semiconductor devices being switched to high impedance internally.

High-density memory modules for use, by way of example, in PCs, workstations and servers, e.g. DDR-DIMMs (double data rate dual in line memory modules), are subject to narrow industrial standards for their dimensions. On the other hand, high-density storage media require as many memory chips as possible to be integrated on the memory module. Reducing the number of components to be integrated on the memory module advantageously results in significant simplification of component placement and the routing of interconnects on the memory module. In memory module configurations commonly used today, the invention advantageously dispenses with between 15 and 31 calibration references.

Since just one calibration reference is now arranged on a memory module at best, on the other hand, more precise implementation of the calibration reference, for example using temperature compensation, is also made possible in addition to simple implementation as a nonreactive resistor or voltage reference.

Calibration of individual or all semiconductor devices arranged to form a data bus system is possible by repeating the above steps 2 to 5 cyclically or as a reaction to an operating condition in the data bus system.

Preferably, the semiconductor devices provided have an instruction evaluation unit which is connected to control and address connections on the semiconductor device, which are provided for connecting a control and address bus. In this case, the calibration signal is generated in the instruction

evaluation unit on the basis of a calibration instruction transmitted via the control and address bus. Performance of the calibration is then controlled by a system which is hierarchically superordinate to the semiconductor device. For data bus systems in which the entire data bus is respectively connected to each of the semiconductor devices arranged to form the data bus system, a packet protocol is executed on the control and address bus and permits individual addressing of each individual semiconductor device. An example of such a data bus system is a fly-by bus.

By contrast, in the case of a hybrid data bus system, the data bus is much wider across the system than a data bus interface on the semiconductor devices.

In this case, sending the calibration instruction exclusively via the control and address bus is no longer sufficient. In line with the invention, this case is catered for by providing for the instruction evaluation units to be provided connected to at least one respective data connection from data connections provided for connecting data lines. The calibration signal is then generated on the basis of a data signal transmitted via the data lines.

On the part of a control chip (busmaster) generating the calibrating instruction, it is necessary to ensure in this context that no more than one semiconductor device is performing the calibration procedure at any time. To this end, either signaling of completed calibration, for example in a mode register in the semiconductor device, or a maximum calibration period required for performing the calibration in a semiconductor device is awaited.

Typically, the inventive calibration method is provided for memory chips having a DDR (double data rate) interface. However, other applications, for example for aligning sensor arrays, are obvious to a person skilled in the art.

Memory chips with a DDR interface have output drivers for outputting data signals on the data lines and/or terminations for low-reflection termination of the data lines (DQ). As a result of the output drivers being aligned, narrower tolerance bands are obtained, e.g. for rise times and response times (slew rate) or else for the turn-on resistance and consequently higher data transmission rates.

In the case of an operating method for a plurality of semiconductor devices which are respectively connected to a common calibration reference and are arranged to form a data bus system having a control and address bus and an at least partially common data bus, the semiconductor devices are calibrated cyclically and/or on the basis of operating states of the data bus system. This is done by transmitting calibration instructions, in each case individually, to the semiconductor devices via the control and address bus (CA) indirectly or directly in succession and performing calibration in the respectively addressed semiconductor device.

If it is insufficient to send the calibration instruction exclusively via the control and address bus on account of the bus configuration, then the invention makes provision for the semiconductor device to be addressed for calibration on the basis of a further data signal transmitted via at least one data signal, data mask or data strobe signal line.

A semiconductor device which is suitable for the calibration method in accordance with the invention has a controllable switching unit in addition to control and address connections for connecting a control and address bus, data connections for connecting a data bus, a calibration connection for connecting a calibration reference, an instruction evaluation unit connected to the control and address connections, and a calibration unit connected to the calibration connection via a calibration path. The controllable switching unit can be used to open and to close the calibration path on the basis of calibration instructions transmitted via the control and address bus to the instruction evaluation unit.

In another embodiment of the inventive semiconductor device, the switching unit can be controlled on the basis of a data signal transmitted via at least one further data line.

Preferably, the semiconductor devices in this case are in the form of DRAMs with a DDR interface.

The advantages of the inventive calibration method and of the inventive semiconductor device relate, in particular, to computer-system memory modules which are fitted with a plurality of semiconductor devices in the form of DDR-DRAMs, in line with the invention. The dimensions and electrical interfaces of the memory modules are subject to industrial standards. In this context, the dimensions of the memory modules are normally minimized, in terms of a standard number of 16 or 32 semiconductor devices per memory module, such that additional components (such as the calibration references) can be placed and wired only with extraordinary difficulty. A memory module in line with the invention now has a single calibration reference instead of 16 or 32 calibration references on the basis of the standard, and this single

calibration reference can also be matched quickly to various installation conditions.

The invention is explained in more detail below with reference to figures, where the same reference symbols are used for components which correspond to one another. In the figures:

Fig. 1 shows a schematic illustration of a conventional semiconductor device,

Fig. 2 shows a schematic illustration of a conventional arrangement,

Fig. 3 shows a schematic illustration of an inventive semiconductor device,

Fig. 4 shows a schematic illustration of an inventive arrangement based on a first exemplary embodiment, and

Fig. 5 shows a schematic illustration of an inventive arrangement based on a second exemplary embodiment.

Figs. 1 and 2 have already been explained at the outset.

The inventive semiconductor device 1 shown in Fig. 3 is a semiconductor memory device with a DDR interface. The semiconductor device has a calibration connection 32 which is connected to an auxiliary potential VP via a calibration reference 5. In addition, control and address connections 21 for connecting a control and address bus CA are provided on the semiconductor device 1. A calibration instruction transmitted via the control and address bus CA is converted by an instruction evaluation unit 2 into a calibration signal which is routed to a switching unit 4 via a calibration signal

path 41. The switching unit 4 is arranged in a calibration path 31. On the basis of the calibration signal, the calibration connection 32 is connected to a calibration unit 3 by means of the switching unit 4 or is without an internal connection.

The calibration unit 3 is either automatic or is activated by the instruction evaluation unit 2 via an auxiliary path 42 (shown in dashes) and aligns output drivers 6 using an auxiliary voltage generated using the calibration reference 5.

To activate the calibration signal, it is also possible to assess data signals, applied to data connections 22, on a data bus DQ, on a data mask bus DM and/or data strobe signals DQS in the instruction evaluation unit 2.

In the arrangement shown in Fig. 4, a plurality of the semiconductor devices 1 shown in Fig. 3 are combined to form a data bus system having a common control and address bus CA and a common data bus DQ. Each semiconductor device 1 is connected to an auxiliary potential VP via a common calibration reference 5. Each semiconductor device 1 can be individually addressed via the control and address bus CA.

In line with the inventive calibration method, the switching units 4 in all the semiconductor devices 1 are initially open and hence the calibration connections 32 in the semiconductor devices 1 are switched to high impedance. A calibration cycle starts to transmit a calibration instruction to a first semiconductor device 1 via the control and address bus CA. In the addressed first semiconductor device 1, the calibration instruction initiates an active calibration signal on the calibration signal path 41. The switching unit 4 in the addressed semiconductor device 1 is closed and the calibration

unit 3 of the addressed semiconductor device 1 is connected to the calibration reference. By way of example, the output drivers or the terminations of the semiconductor device 1 are then calibrated.

After a calibration period has elapsed, the switching unit is opened. The switching unit 4 is opened under time control when a timer has run out, using an output signal from the calibration unit 3 (calibration complete) or by a control instruction transmitted via the control and address bus. If it is certain that the calibration connection 32 on the first semiconductor device 1 has been switched to high impedance, that is to say either after the calibration period has elapsed or as a result of the calibration state being read from a mode register in the instruction evaluation unit, a further calibration instruction is sent to a second semiconductor device.

In a fly-by data bus system as shown in Fig. 4, data bus interfaces in the semiconductor devices 1 each have the same width, that is to say an identical number of data signal lines, and can always be addressed individually. To send the calibration instruction explicitly, the control and address bus CA is thus sufficient in each case.

In hybrid data bus systems, in which just some of the data signal lines are routed to the semiconductor devices 1 in each case, the control and address bus CA respectively addresses a plurality of semiconductor devices 1 simultaneously. Thus, by way of example, the DDR bus concept provides a data bus width of 64 bits, while the number of data bus connections on the semiconductor devices 1 provided for the DDR bus concept is limited to 16 bits. In such a hybrid data bus system, four

semiconductor memory devices 1 are addressed simultaneously when a data address is accessed.

To assign a calibration instruction explicitly to one of these semiconductor memory devices 1, in addition to the addressing in the control and address bus CA, further information is used from a data bus DQ, a data mask bus DM or the data strobe signals DQS. In the exemplary embodiment shown in Fig. 5, this purpose is served by providing, by way of example, the data signal lines DQ[0] for the bottom semiconductor device, DQ[16] for the one arranged above that, DQ[32] for the next and DQ[48] for the top semiconductor device.

Patent Claims

1. A method for calibrating interface devices (6) in semiconductor devices (1) using a calibration reference (5) which is connected to at least one calibration connection (32) on a semiconductor device (1), comprising the following steps:
1) a plurality of semiconductor devices (1) which each have a calibration unit (3) which is connected to the calibration connection (32) via a calibration path (31) which can be switched by a switching unit (4) are provided,
2) an active calibration signal connecting the calibration unit (3) to the calibration connection (2) using the switching unit (4) is respectively generated in a first semiconductor device (1),
3) the interface devices (6) in the first semiconductor device (1) are calibrated,
4) a passive calibration signal isolating the calibration unit (3) from the calibration connection (32) using the switching unit (4) is generated, and
5) steps 2) to 4) are respectively repeated for all further semiconductor devices (1).

2. The calibration method as claimed in claim 1, characterized
in that steps 2) to 5) are repeated cyclically or as a reaction to an operating condition in one of the semiconductor devices (1).

3. The calibration method as claimed in either of claims 1 and 2,
characterized
in that the semiconductor devices (1) are respectively provided with an instruction evaluation unit (2) which is connected to control and address connections (21) on the

semiconductor device (1) which are provided for connecting a control and address bus (CA), and the active calibration signal is generated in the instruction evaluation unit (2) on the basis of a calibration instruction transmitted via the control and address bus (CA).

4. The calibration method as claimed in claim 3, characterized
in that the instruction evaluation units (2) are provided connected to at least one respective data connection (22) provided for connecting a data line (DQ, DM, DQS), and the active calibration signal is generated on the basis of a data signal transmitted via the data line (DQ, DM, DQS).

5. The calibration method as claimed in one of claims 1 to 4, characterized
in that the semiconductor devices (1) provided are memory chips having a DDR (double data rate) interface.

6. The calibration method as claimed in one of claims 1 to 5, characterized
in that the interface devices (6) to be calibrated which are provided are output drivers for outputting data signals on data signal lines (DQ) and/or terminations for low-reflection termination of the data signal lines (DQ).

7. A method for operating a plurality of semiconductor devices (1) which are respectively connected to a common calibration reference (5) and are arranged to form a data bus system having a control and address bus (CA) and having an at least partially common data bus (DQ),
characterized
in that calibration instructions are transmitted, in each case individually, to the semiconductor devices (1) via the control

and address bus (CA) in indirect or direct succession cyclically and/or on the basis of operating states of the data bus system, a calibration connection (32) is connected to a calibration unit (3) in the respectively addressed semiconductor device (1), interface devices (6) in the addressed semiconductor device (1) are calibrated using the calibration unit (3), and after the calibration the calibration connection (32) is switched to high impedance.

8. The operating method as claimed in claim 7, characterized
in that the semiconductor device (1) is addressed for calibration on the basis of a data signal transmitted via at least one further data line (DQ, DM, DQS).

9. A semiconductor device having control and address connections (21) for connecting a control and address bus (CA), having data connections (22) for connecting a data bus (DQ), a calibration connection (32) for connecting a calibration reference (5), an instruction evaluation unit (2) connected to the control and address connections (21), and a calibration unit connected to the calibration connection (32) via a calibration path (31),
characterized by
a switching unit (4) which opens or closes the calibration path (31) and can be controlled via a calibration signal path (41) using the instruction evaluation unit (2) on the basis of calibration instructions transmitted via the control and address bus (CA).

10. Semiconductor device as claimed in claim 9, characterized in that

the switching unit (4) can be controlled on the basis of a data signal transmitted via at least one data line (DQ, DM, DQS).

11. The semiconductor device as claimed in either of claims 9 and 10,
characterized
in that the semiconductor devices (1) are in the form of memory chips and each have a DDR (double data rate) interface.

12. The semiconductor device as claimed in one of claims 9 to 11,
characterized by
output drivers which can be calibrated using the calibration unit (5) for the purpose of outputting data signals on data signal lines (DQ) and/or calibratable terminations for terminating the data signal lines (DQ).

13. A memory module for computer systems,
characterized by
a plurality of semiconductor devices (1) as claimed in one of claims 9 to 12.

Abstract

Calibration of semiconductor devices using a common calibration reference

Interface parameters for a plurality of semiconductor devices (1), particularly parameters for output drivers (6) (OCD, on chip driver) and terminations (ODT, on die termination) for DDR-DRAMs (double data rate dynamic random access memories), are aligned using a calibration reference (5) which is common to the semiconductor devices (1) and is connected to calibration connections (32) on the semiconductor devices (1), with the semiconductor devices (1) being calibrated in succession, in each case individually, and the calibration connection (32) on the respective semiconductor device (1) which is currently performing calibration being connected to an internal calibration unit (3) by means of an internal switching unit (4) in the process, and the calibration connections (2) on all other semiconductor devices (1) being terminated at high impedance internally.

(Fig. 4)

List of reference symbols

1 Semiconductor device
1' Semiconductor device
2 Instruction evaluation unit
21 Control and address connections
22 Data connections
3 Calibration unit
31 Calibration path
32 Calibration connection
4 Switching unit
41 Calibration signal path
42 Auxiliary path
5 Calibration reference
6 Output driver
CA Control and address bus
DQ Data bus
DM Data mask bus
DQS Data strobe signals
VP Auxiliary potential